ABSTRACT

The present invention is directed to a transceiver configured for use with a multi-tier system bus that allows for the flow of information to be managed among plural processors by connecting processors within modules on a local bus, which is then connected to the system bus by way of a gateway. The transmitter portion of the transceiver of the present invention allows for the high performance of the bus by providing buffering and interleaved output of direct memory access and control actions packet types. The receiver portion of the transceiver of the present invention provides input discrimination and individual buffering of direct memory access and interrupt control actions packets along with specialized control functions, such as reset, timer, broadcast, and so forth.